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Description

The LC03-3.3 is a 3.3V low capacitance TVS array, combining a TVS diode with a rectifier bridge to provide both common and differential transient protection in one package, The LC03-3.3 complies with the IEC 61000-4-2 (ESD) with \pm 30kV air and \pm 30kV contact discharge. It is assembled into a 8-pin lead-free SO-8 package, the LC03 -3.3 is rated for GR-1089, intra-building transient immunity requirements for telecommunication installations and provide overvoltage protection for applications such as 10/100/1000 BaseT Ethernet and T3/E3 interfaces.

Features

- Low capacitance for high speed interfaces
- Ultra low leakage: nA level
- Low operating voltage
- Low clamping voltage
- Protects two lines in common and differential mode
- JEDEC SO-8 package
- Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test
 Air discharge: ±30kV
 Contact discharge: ±30kV
 - IEC61000-4-5 (Lightning) 100A (8/20µs)
- RoHS Compliant

Mechanical Characteristics

- Package: SO-8
- Lead Finish: Matte Tin
- Case Material: "Green" Molding Compound.
- Terminal Connections: See Diagram Below
- Marking Information: See Below

Applications

- T1/E1 Line Cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet
- ISDN Interfaces
- Low Voltage Interfaces



SOP-8



Circuit diagram



Dot denotes Pin1

Ordering Information

Part Number	Packaging	Reel Size	
LC03-3.3	2500/Tape & Reel	13 inch	

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20µs)	Ppk	1800	W
Peak Pulse Current (8/20µs)	IPP	100	А
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	Vesd	±30 ±30	kV
Operating Temperature Range	TJ	−55 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min	Тур	Мах	Unit	Test Condition
Reverse Working Voltage	VRWM			3.3	V	Any I/O Pin to GND
Punch-Through Voltage	Vpt	3.5			V	Iτ = 2μA, any I/O Pin to GND
Snap-Back Voltage	Vsв	2.8			V	IT = 50mA, any I/O Pin to GND
Reverse Leakage Current	I _R			1	μA	VRWM = 3.3V, any I/O Pin to GND
Clamping Voltage	Vc			11	V	IPP = 50A (8 x 20µs pulse), any I/O Pin to GND
Clamping Voltage	Vc			13	V	IPP = 50A (8 x 20µs pulse), between I/O Pins
Clamping Voltage	Vc			15	V	IPP = 100A (8 x 20µs pulse), any I/O Pin to GND
Clamping Voltage	Vc			18	V	IPP = 100A (8 x 20µs pulse), between I/O Pins
Junction Capacitance	Сл		9	12	pF	VR = 0V, f = 1MHz, any I/O Pin to GND
Junction Capacitance	Сл		4.5	6	pF	VR = 0V, f = 1MHz, between I/O Pins

Note 1: I/O Pins are Pin 1, 4, 5 and 8

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Typical Application

The LC03-3.3 is designed to protect two high speed data lines (one differential pair) from transient over-voltages which result from lightning and ESD. The device can be configured to protect in differential (Line to Line) and common (Line to Ground) mode. Data line inputs/outputs are connected at pins 1 to 8, and 4 to 5 as shown below. Pins 2, 3, 6, 7 are connected to ground. These pins should be connected directly to a ground plane on the board for the best results, the path length is kept as short as possible to minimize parasitic inductance. In applications where high common voltages are present, differential protection is achieved by leaving pins 2, 3, 6, and 7 not connected.



Connection for differential (Line to Line) and common mode protection (Line to Ground)



Connection for differential protection (Line to Line)

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LC03-3.3

SOP-8 Package Outline Drawing







Symbol	Dimensions In	Millimeters	Dimensions In Inches		
	Min	Max	Min	Max	
А	1.350	1.750	0.053	0.069	
A1	0.100	0.250	0.004	0.010	
A2	1.350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
с	0.170	0.250	0.007	0.010	
D	4.800	5.000	0.189	0.197	
e	1.270 (BSC)		0.050 (BSC)		
Е	5.800	6.200	0.228	0.244	
E1	3.800	4.000	0.150	0.157	
L	0.400	1.270	0.016	0.050	
θ	0°	8°	0 °	8°	

SOP8 Suggested Pad Layout



Note:

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Controlling dimension:in millimeters.
 General tolerance:± 0.05mm.
 The pad layout is for reference purposes only.